In the Claims:

Please amend claims 2, 3, 5, 7, 14-23 and 27-29. Please cancel claims 1, 4, 6, 8-13, 15, 18, 20, 22-30. Please add new claims 31 -36. The claims are as follows:

1. (Canceled)

2. (Currently Amended) The computer system of claim [[1]] 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to ~~one of said~~ a respective I/O driver models.

3. (Currently Amended) The system of claim [[1]] 31, wherein said simulated external memory mapped test device further includes [[an]] a simulated address register.

4. (Canceled)

5. (Currently Amended) The system of claim 2, wherein each said simulated external memory mapped test device module further includes [[an]] a simulated address register.

6. (Canceled)

7. (Currently Amended) The system of claim [[1]] 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated

external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to ~~one of said~~ a respective I/O driver model[[s]] of said one or more I/O driver models and further including the method steps of :

loading code representing an additional simulated external memory mapped test device module into said memory unit;

~~directly connected to~~ said loading of said test case connecting one or more additional I/O driver models to said additional simulated external memory mapped test device by additional simulated I/O buses ~~, each~~ ; and

said loading of said test case connecting each additional I/O driver model ~~directly connected~~ to ~~an~~ a respective additional simulated I/O core by said simulated system bus, each additional simulated I/O core ~~part of~~ comprising said model of integrated circuit design.

8-13 (Canceled)

14. (Currently Amended) A method for verifying an integrated circuit design comprising:

providing a[[n]] simulated I/O controller connected to one or more simulated I/O cores, said simulated I/O cores part of said integrated circuit design;

providing a[[n]] simulated external memory mapped test device having a simulated switch for selectively connecting one or more of said simulated I/O cores to corresponding simulated I/O driver models;

providing a simulated bus for transferring simulated signals between said simulated I/O controller and said simulated switch;

providing a test operating system for allocating I/O pins of said simulated I/O controller and for ~~controlling~~ connecting said simulated switch to said external memory mapped device and to simulated I/O driver models; and

simulating said integrated circuit design by running a test case on said test operating system~~;~~

~~distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said plurality of external memory mapped test device modules I/O driver models; and~~

~~providing an additional external memory mapped test device module directly connected to one or more additional plurality of external memory mapped test device modules I/O driver models, each additional plurality of external memory mapped test device modules I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design~~.

15. (Canceled)

16. (Currently Amended) The program storage device of claim [[15]] 32, said method steps further including:

distributing said simulated external memory mapped test device and said simulated switch among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory modules containing a portion of said simulated switch and connected to one of said simulated I/O driver models.

17. (Currently Amended) The program storage device of claim [[15]] 32, said method steps further including:

providing said simulated external memory mapped test device with [[an]] a simulated address register; and setting said simulated switch and controlling said simulated I/O driver using address information programmed into said simulated address register.

18. (Canceled)

19. (Currently Amended) The program storage device of claim 16, said method steps further including:

providing each simulated external memory mapped test device with [[an]] a simulated address register; and

setting each portion of said simulated switch and controlling each simulated I/O driver using address information programmed into said simulated address register.

20. (Canceled)

21. (Currently Amended) The computer system of claim [[1]] 31, wherein said one or more simulated I/O cores ~~are independently selected from the group consisting of~~ includes a simulated 1394 I/O core[[s]], a simulated universal asynchronous receiver transmitter core[[s]], a simulated serial cores, ~~and~~ a simulated general purpose I/O core[[s]], a direct memory access core or combinations thereof.

22 -30 (Canceled)

28 -30. (Canceled)

31. (New) A computer system comprising a processor and a computer-readable memory unit coupled to communicate with said processor, said memory unit containing instructions that when executed by the processor implement a method for verifying an integrated circuit design, said method comprising the computer implemented steps of:

loading code representing said integrated circuit design into said memory unit, said integrated circuit design including simulated I/O cores, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus;

loading code representing an external memory model, a simulated external memory mapped test device and one or more I/O driver models into said memory unit, said simulated external memory mapped test device including a simulated switch programmably connectable to said one or more I/O driver models, to said simulated I/O controller and to said external memory model, said I/O driver models connected to corresponding said simulated I/O cores by corresponding simulated I/O buses;

loading a test case comprising a list of computer-executable instructions on said simulated processor, said loading of said test case allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said

simulated external memory mapped test device to said simulated I/O controller and to said one or more of said simulated I/O cores;

executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case; and

outputting said data representing a response of said computer simulation model of said integrated circuit design to said test case.

32. (New) A program storage device readable by machine, tangibly embodying a program of instructions executable by machine to perform method steps a method for verifying an integrated circuit design, said method steps comprising:

generating a model of said integrated circuit design, said integrated circuit design including simulated I/O cores, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus;

generating an external memory model, a simulated external memory mapped test device and one or more I/O driver models, said simulated external memory mapped test device including a simulated switch programmably connectable to said one or more I/O driver models, to said simulated I/O controller and to said external memory model, said I/O driver models connected to corresponding said simulated I/O cores by corresponding simulated I/O buses;

loading a test case comprising a list of computer-executable instructions on said simulated processor, said loading of said test case allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said

simulated external memory mapped test device to said simulated I/O controller and to said one or more of said simulated I/O cores; and

executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case.

33. (New) The method of claim 14, further including:

distributing said simulated external memory mapped test device and said simulated switch among a plurality of simulated external memory mapped test device modules, each simulated external memory mapped test device module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to one of said plurality of simulated external memory mapped test device modules I/O driver models: and

providing an additional simulated external memory mapped test device module directly connected to one or more additional plurality of simulated external memory mapped test device modules I/O driver models, each additional plurality of simulated external memory mapped test device modules I/O driver model of said additional plurality of simulated external memory mapped test device modules directly connected to an additional simulated I/O core, each additional simulated I/O core part of said integrated circuit design.

34. (New) The method of claim 14, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory

mapped test device modules containing a portion of said simulated switch and connected to respective I/O driver models.

35. (New) The method of claim 14, wherein said simulated external memory mapped test device further includes a simulated address register.

36. (New) The method of claim 14, wherein each said simulated external memory mapped test device module further includes a simulated address register.